Novel Transistor Concepts Based on 2D Systems- Graphene and Topological Insulators
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Beyond-CMOS device concept- the BiSFET
Graphene Tunnel FETs
Topological Insulators

Acknowledgments: NRI SWAN (UT, UTD, Rice, A&M, UMD, NCSU); DARPA CERA
Pseudospintronics in Bilayers at low T, high B

- Charge-neutral superfluid: Bose-Einstein condensate of excitons!
- Electron-hole pairing $\Rightarrow$ enhanced interlayer conductance with NDR

Pseudospintronics in Graphene Double Layers?

- Particle-Hole Symmetric
- Low density of states $n = p = \frac{(E_F\hbar v)^2}{\pi} = 5\times10^{12}/\text{cm}^2$ for $E_F = 10k_B(300 \text{ K})$
- Gapless
- Truly 2D
Bi-layer pseudoSpin Field Effect Transistor (BiSFET)

SPICE™ model details for “trial” BiSFET

- $T_c = 300 \text{ K}$
- $t_{\text{gate ox,eff.}} = 1 \text{ nm (high k)}$  
  $\rightarrow C_G = 3.5 \times 10^{-6} \text{ F/cm}^2$
- $t_{\text{tunnel ox,eff.}} = 1 \text{ nm (low k?) }$  
  $\rightarrow C_{il} = 3.5 \times 10^{-6} \text{ F/cm}^2$
- $E_F = 10 k_B T_c = 259 \text{ meV} \rightarrow n_o = p_o = 4.9 \times 10^{12}/\text{cm}^2  \rightarrow C_Q = 6.1 \times 10^{-6} \text{ F/cm}^2$
- $= q^2(\partial n/\partial E_F) = 2q^2E_F/(\pi\hbar^2v^2)$ (→ e.g., effective gate work functions relative to graphene Dirac point of $\phi_{G,n/p} = \pm 1 \text{ eV}$)
- unity peak transmission probability $\rightarrow G_0 = 4e^2k_F/(\pi\hbar) = G_0 = 195 \text{ ohm}^{-1}\text{cm}^{-1}$
- $\Delta_o = 2 \text{ meV} \rightarrow \lambda_j \approx 8 \text{ nm} \rightarrow \text{gate length} = 10 \text{ nm and } I_{\text{max, o}} = 125 \mu\text{A/\mu m}$
  $= e\rho_s/(\hbar\lambda_j) \approx e k_B T_c / (\hbar \lambda_j) \rightarrow V_{\text{max, o}} = 6.4 \text{ mV} = I_{\text{max, o}}/G_0$
- $V_{\text{max}} = V_{\text{max, o}} \exp(-10 | \Delta p - \Delta n | / (n + p))$
- $I = G_0 (V_p - V_n) \left[1 + \left(\frac{(V_p - V_n)/V_{\text{max}}}{\exp(1 - |V_p - V_n| / V_{\text{max}})}\right)^4\right]^{-4}$
How *not to* use BiSFET characteristics for logic:

BiSFET-based inverter

\[ V_{dd} = 25 \text{ mV} \]

\[ V_{\text{in}} = -25 \text{ mV} \]

\[ \frac{W}{L} = 2 \]

Load Line Plot for Inverter

Translucent Simulation of a Inverter
How to use BiSFET characteristics for logic: BiSFET-based inverter *with clocked supply*

\[
V_{dd,\text{max}} = 25 \text{ mV}
\]

100 GHz SPICE™ simulation

Load Line Plot for Inverter

Transient Simulation of an Inverter

\[
V = -25 \text{ mV}
\]

\[
2L = W
\]

\[
V_{dd} \text{ and } V_{out} [\text{mV}]
\]

\[
V_{dd} \text{ and } V_{out} [\text{mV}]
\]

\[
\text{Time [ps]}
\]
1.0 nm EOT, gate $L=10$ nm, corresponding to the Josephson length, and $W=20$ nm. Clock frequency = 100 GHz and $V_{\text{clock,peak}} = 25$ mV with 2.5 ps rise time. Input and output signals were subject to a fan-in and fan-out of 4 inverters. Current MOSFETs consume $\sim100$ aJ per switching and 2020 “end of the roadmap CMOS will consume 5 aJ [www.itrs.net]. Energy consumed per switching operation per BiSFET = 0.008 aJ! (2X Landauer limit)
Clock:
- V_{low} = 0 mV; V_{high} = 25 mV
- Rise time = 2.5 ps
- Fall time = 2.5 ps
- Pulse width = 2.5 ps
- Pulse period = 10 ps
- Frequency of clock = 100 GHz
- Delay between clock and input signal is 2.5 ps

- Maximum number of inverters the OR gate can drive: 6
- Energy per operation:
  - For OR GATE (load = 4 inverters) total energy for 4 operations: \(133.7 \times 1E-21 \text{ J}\)
  - Average Energy per operation: \(33.4 \times 1E-21 \text{ J}\)
  - For NAND GATE (load = 4 inverters) total energy for 4 operations: \(121.81 \times 1E-21 \text{ J}\)
  - Average Energy per operation: \(30.45 \times 1E-21 \text{ J}\)
Input output characteristics and power consumption of BiSFET-NAND/OR gate

100 GHz SPICE™ NAND gate simulation with four-inverter fan-in and fan-out

100 GHz SPICE™ OR gate simulation with four-inverter fan-in and fan-out

energy consumed per switching operation per NAND gate = 0.030 aJ; energy consumed per switching operation per OR gate = 0.033 aJ
Elements of a BiSFET (but not a fabrication scheme)

gate dielectric: perhaps high-k for increased gate control; perhaps ferroelectric to induce required sheet charge layers in graphene under zero gate bias.

Gates: used to control charge densities in graphene layers; perhaps work-function engineered to provide required sheet charge densities under zero bias.

tunnel barrier: perhaps dielectric … or just misaligned bilayers?

Perhaps one gate used as only a “backgate” with fixed voltage/workfunction to provide required sheet charge densities under zero bias.
FETs on Large-Area Graphene Grown on Cu Foils

Large-Area Synthesis of High-Quality and Uniform Graphene Films on Copper Foils
Xuesong Li\textsuperscript{a}, Weiwei Cai\textsuperscript{a}, Jinho An\textsuperscript{a}, Seyoung Kim\textsuperscript{b}, Junghyo Nah\textsuperscript{b}, Dongxing Yang\textsuperscript{a}, Richard Piner\textsuperscript{a}, Aruna Velamakanni\textsuperscript{a}, Inhwa Jung\textsuperscript{a}, Emanuel Tutuc\textsuperscript{b}, Sanjay K. Banerjee\textsuperscript{b}, Luigi Colombo\textsuperscript{c*, Rodney S. Ruoff\textsuperscript{a*}. Science, 2009
Fabrication process of independently-contacted bilayer device

※ Scale bar: 10um
Coulomb drag in Bilayer Graphene (Tutuc) originates from interlayer e-e interactions - a sensitive tool to probe the ground states of the system.

Drag resistivity should jump to a value comparable to the isolated layer resistivity (kOhms) if a condensate forms. Drag data so far is consistent with Fermi liquid theory, except for mesoscopic fluctuations at low temp.

2D-to-2D Tunnel FETs in Graphene

\[
\begin{align*}
Q_1 (\zeta_1) &= - \left( C_{g1} 0 \begin{array}{c} V_{g1} - V_{FB1} - \frac{\zeta_1}{e} - V_1 \\ V_{g2} - V_{FB2} - \frac{\zeta_2}{e} - V_2 \end{array} \right) \\
&\quad + \left( C_{d1} - C_{d1} \begin{array}{c} \frac{\zeta_1}{e} + V_1 \\ \frac{\zeta_2}{e} + V_2 \end{array} \right) \\
Q_2 (\zeta_2) &= \left( C_{g2} \right) \\
&\quad + \left( C_{d2} - C_{d2} \right)
\end{align*}
\]

\[
H = \sum_{k_s} \varepsilon_{1k_s} a_{1k_s}^{\dagger} a_{1k_s} + \sum_{k_s} \varepsilon_{2k_s} a_{2k_s}^{\dagger} a_{2k_s}
+ \frac{1}{2} \sum_k t_k (a_{1ck}^{\dagger} - b_{1vk}^{\dagger}) (a_{2ck} + b_{2vk}) + h.c
\]

\[
I = -\frac{q}{h} \int_{-\infty}^{\infty} T(E) \left[ f(E - \mu_1) - f(E - \mu_2) \right] \frac{dE}{2\pi}
\]

\[
T(E) = \sum_{k;ss'} |t_k|^2 A_{1s} (k, E) A_{2s'} (k, E)
\]
DC Characteristics of Graphene Tunnel FET

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Value</th>
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<tr>
<td>$\Gamma$</td>
<td>2 meV</td>
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<tr>
<td>$t$</td>
<td>2 meV</td>
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<tr>
<td>$m^*$</td>
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<tr>
<td>$N_0$</td>
<td>$1.8 \times 10^{16}$ m$^{-2}$</td>
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<tr>
<td>$T$</td>
<td>300 K</td>
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<tr>
<td>$L$</td>
<td>10 nm</td>
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<tr>
<td>$W$</td>
<td>20 nm</td>
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<tr>
<td>$t_{ox}$</td>
<td>1 nm</td>
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</table>
Modeling Interlayer Tunneling Resistance

• Modeling
  – Comsol Multiphysics 4.0 – FEM software
  – Set resistivity using extracted characteristics
  – Introduce boundary conditions
  – Insert a constant contact resistance between layers

• Specific resistance
  – Low: 2.25 x 10^{-5} \Omega \text{cm}^2
  – High: 7.5 x 10^{-5} \Omega \text{cm}^2
Bi$_2$Se$_3$ TI based TFETs

Possible Applications of TI Thin Films for Tunnel FETs, Chang, Register, Banerjee, DRC 2012
Dielectric capping effects on binary and ternary TI surface states, Chang, Jadaun, Register, Banerjee, Sahu, PRB, 2011
What is needed in the new switch?

**CMOS ca 2020**
- Energy ~ 5 aJ/op; power~ $10^7$ W/cm²
- Speed ~ 0.1 ps/op (10 THz $f_T$; 100 GHz circuit)
- Size ~ $L_g$ 5 nm; cell ~ 100 nm, $I_{DN}$ ~ 3 mA/µm
- Density ~ $10^{10}$ cm⁻²; BIT ~100 GBit/ns/cm²
- Cost ~ $10^{-12}$ $$/gate

**Desirable Attributes**
- Energy efficiency 0.01 aJ/op
- Speed (performance, noise) 100 GHz
- Room T operation (non-equilibrium devices?) Yes
- Size (device/ wafer): capacitance, fan-out 10 nm, FO=4
- Gain; uni-directional signal flow (I/O isolation) Yes
- Reliability, manufacturability, cost ???
- CMOS compatibility (process, topology) ???

**Speed = CV/I**

**Active Power = CV²f**

**Stand-by Power = Sub-$V_T$, gate leakage**
Top- and Bottom-graphene Resistance Modeling

Equivalent Circuit model with $C_Q$

$\nu = \frac{E_F}{e} + \frac{ne}{C_{ox}}$

$C_Q = 2e^2 \frac{\sqrt{n}}{\hbar v_F \sqrt{\pi}}$

Repeat until $|V_1 - V_1'| \approx 0$
Subthreshold leakage is diffusion current from S to D (as in BJT)

\[ S = \ln 10 \frac{kT}{q} \left( 1 + \frac{C_d}{C_{ox}} \right) \]
Classic Distinguishability: The Boltzmann constraint

How small can the energy barrier height be?

Barrier control (gate)

$E_{bit}^{\text{min}} = E_b$

Distinguishability requirement: The probability of spontaneous transitions (errors) $\Pi_{\text{error}} < 0.5$ (50%)

$\Pi_{\text{error}} = \exp\left(-\frac{E_b}{k_B T}\right)$

$0.5 = \exp\left(-\frac{E_b}{k_B T}\right)$

$E_b^{\text{min}} = k_B T \ln 2$
Quantum Distinguishability: The Heisenberg Constraint

\[ a_{\text{crit}} = \frac{\hbar}{\sqrt{2mE_b}} \]

\[ E_{b, \text{min}} \sim \frac{\hbar^2}{2ma^2} \]

Wigner-Kramers-Brillouin (WKB) approximation for tunneling:

\[ \Pi_{\text{quantum}} = \exp\left(-\frac{2\sqrt{2m}}{\hbar} \cdot a \sqrt{E_b}\right) \]

\[ E_{b, \text{min}} = \frac{\hbar^2 \ln^2 2}{8ma^2} \quad (\text{at } \Pi=0.5) \]
What Else Could be Done? – Explore new approaches

◆ “Different” spintronics
  (1) Can we make spin devices that operate without moving electrons?
  (2) Non-equilibrium operation of binary switch?

◆ Orbitronics
  Interplay between charge, orbital, and spin degrees of freedom. Materials with both ferroelectricity and ferromagnetism (electrically controlled)
  (1) Can we move atoms instead of moving electrons?

◆ Phononics: thermal breakthrough
  (1) How can we better remove heat and what are the fundamental limits of heat removal?
  (2) How can we isolate selected materials subsystems from thermal noise?
  (3) Are there ways to control phonon movement by external stimuli.
  *Co-design of electric and thermal circuits?*

◆ Invent high speed, high density, *electrically accessible*, non-volatile memory.
1) Minimum energy per binary transition

\[ E_{\text{bit}}^{\text{min}} = k_B T \ln 2 \]

2) Minimum distance between two distinguishable states (Heisenberg)

\[ \Delta x \Delta p \geq \hbar \]
\[ x_{\text{min}} = a = \frac{\hbar}{\sqrt{2mkT \ln 2}} = 1.5 \text{nm} (300K) \]

3) Minimum state switching time (Heisenberg)

\[ \Delta E \Delta t \geq \hbar \]
\[ t_{st} = \frac{\hbar}{kT \ln 2} = 4 \times 10^{-14} \text{s} (300K) \]

4) Maximum gate density

\[ n = \frac{1}{x_{\text{min}}^2} = 4.6 \times 10^{13} \frac{\text{gate}}{\text{cm}^2} \]

\[ P_{\text{chip}} = \frac{n \cdot E_{\text{bit}}}{t} = 4.6 \cdot 10^{13} \text{[cm}^{-2}] \cdot \frac{3 \cdot 10^{-21} \text{[J]}}{4 \cdot 10^{-14} \text{[s]}} \]

\[ E_{\text{bit}} = k_B T \ln 2 \approx 3 \cdot 10^{-21} \text{J} \]

\[ P_{\text{chip}} = 4.74 \times 10^6 \frac{W}{\text{cm}^2} \quad \text{T}=300 \text{ K} \]

Cavin, Hutchby, Zhirnov, Bourianoff
**The Scale of Things – Nanometers and More**

**Things Natural**

- Ant ~5 mm
- Dust mite ~200 μm
- Human hair ~60-120 μm wide
- Fly ash ~10-20 μm
- Red blood cells with white cell ~2-5 μm

**DNA**

- ~2-1/2 nm diameter
- Atoms of silicon spacing ~tenths of nm

**Things Manmade**

- Head of a pin 1-2 mm
- MicroElectroMechanical (MEMS) devices 10-100 μm wide
- Red blood cells
- Pollen grain
- Quantum corral of 48 iron atoms on copper surface positioned one at a time with an STM tip

**Microworld**

- 1 cm
- 10 mm
- 1,000,000 nanometers = 1 millimeter (mm)
- 100 μm
- 0.1 mm
- 0.01 mm
- 10 μm
- 1 μm
- 0.1 μm
- 100 nm
- 0.01 μm

**Nanoworld**

- 1 nanometer (nm)
- 1,000 nanometers = 1 micrometer (μm)
- 100 nm
- 10 nm
- 1 nm

**Visible**

- 1,000,000 nanometers = 1 millimeter

**Microwave**

- Infrared
- Ultraviolet
- Soft x-ray

**More is different!**

**Smaller is different!**

**The Challenge**

Fabricate and combine nanoscale building blocks to make useful devices, e.g., a photosynthetic reaction center with integral semiconductor storage.
Quantum 2-Level Systems

cos(\theta/2) + sin(\theta/2) e^{i\varphi}

\{ top layer: \uparrow \}
\{ bottom layer: \downarrow \}

cos(\theta/2) + sin(\theta/2) e^{i\varphi}

\text{top layer:} \uparrow \
\text{bottom layer:} \downarrow
Electron Spin Precession in Magnetic Field

Spin dynamics analogous to 2-state system -> Pseudospin

$$\begin{pmatrix} H_{11} & H_{12} \\ H_{21} & H_{22} \end{pmatrix}$$

$$H = -\mu \cdot B = \begin{pmatrix} -\mu B_z & -\mu(B_x - iB_y) \\ \mu(B_x + iB_y) & +\mu B_z \end{pmatrix}$$

Polar angles $$(\theta, \varphi)$$
**Pseudo-spintronic devices**

- Device consisting of two electron and/or hole layers in close proximity

![Diagram showing two layers with electrons and holes](image)

\[ \Psi_{\nu=1} = \Psi_{111} \sim \prod_{i<j} (z_i - z_j) \prod_{i<j} (w_i - w_j) \prod_{i,j} (z_i - w_j) \]

- Inter-layer electron-electron interaction strong \( \Rightarrow \) “layer” (pseudo-spin) degree of freedom uncertain

- Charge transport intimately determined by the dynamics of the pseudo-spin degree of freedom
Interlayer *electron-hole* tunneling/recombination between oppositely-charged graphene bi-layers (with or without exciton condensate)

\[ V_{\text{top, left}} \]

\[ \varphi_{\text{hole}} \rightarrow \varphi_{\text{electron}} \rightarrow (I_{\text{hole}} \rightarrow) \]

\[ V_{\text{bottom, left}} \]

\[ \varphi_{\text{electron}} \rightarrow (I_{\text{electron}} \leftarrow) \]

- uncoupled “leads”
- coupled “channel”

- Electron hole recombination via tunneling
- Evanescent states only in gap

\[ E \]

\[ k \]
Allotropes of Carbon

a) diamond  b) graphite  c) lonsdaleite
d) $C_{60}$  e) $C_{540}$  f) $C_{70}$
g) amorphous  h) SWCNT

Mother Nature
4B Years ago

Buckyballs, 1985

Iijima, 1991

Geim, 2004
Nobel Prize, 2010

FIG. 1. Ternary phase diagram of amorphous carbons. The three corners correspond to diamond, graphite, and hydrocarbons, respectively.
BiSFET vs. MOSFET and gated RTD’s characteristics

- **BiSFET**
  
  Peak conductivity centered at $V_p-V_n = 0$

  \[ |V_{G,p} - V_{G,peak}| = 0 \]

  \[ |V_{G,p} - V_{G,peak}| = k_B T_C \]

  \[ V_{\text{max}} < k_B T_C \]

- **Gated-RTD**
  
  Location of peak conductivity varies with $V_G$
Signal restoration in inverter

$V_{dd, max} = 25 \text{ mV}$

100 GHz SPICE™ simulation with fan-in and fan-out of two inverters

$V = -13.5 \text{ mV}$
Noise and Jitter Studies

100 GHz Clock, Td_Min = 1.5p

100 GHz Clock, Td_Max = 4.5p

67 GHz Clock, Td_Min = 1.5p

67 GHz Clock, Td_Max = 6.0p

Clock     Min_Td  Nom_Td  Max_Td
100 GHz   1.5 ps  3.0 ps  4.5 ps
67 GHz     1.5 ps  3.75 ps 6.0 ps
One bit full adder

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1-Bit Adder Simulation (Hassibi)

- 1-bit Full Adder Test (w/ PLL output and a “weak” level shifter)
How to use BiSFET characteristics for storage: 
BiSFET-based Memory

quasi-static (100 KHz SPICE™ simulation))

Load Line Plot for Inverter

Transient Simulation of a Inverter

$V_{dd} = 25 \text{ mV}$

$V = -25 \text{ mV}$
Modeling Approach: Single Particle Tunneling

\[ H = H_T + H_2 + H_1 \]

Linear Response

\[ I = \langle \frac{dN}{dt} \rangle = i[H, N] \]

Hamiltonian in Second Quantization Representation

\[ H_1 = \sum_{nk} \epsilon_{nk1} c_{nk1}^\dagger c_{nk1} \]

\[ n \text{ is band index} \]

\[ k \text{ is Bloch momentum} \]

\[ T \text{ is tunneling matrix} \]

\[ H_2 = \sum_{nk} \epsilon_{nk2} c_{nk2}^\dagger c_{nk2} \]

\[ H_T = \sum_{kk', nn'} T_{nk,n'k'} c_{nk1}^\dagger c_{n'k'2} + T_{n'k',nk} c_{n'k'2}^\dagger c_{nk1} \]

\[ I = \int_{-\infty}^{\infty} \frac{d\omega}{2\pi} \sum_{kk', nn'} \left| T_{nk,n'k'} \right|^2 A_1(nk, \omega) A_2(n'k', \omega + eV) \left[ n_F(\omega + eV) - n_F(\omega) \right] \]

\[ A_1(nk, \omega) = \frac{2\Gamma}{(\omega - \epsilon_{nk1} + \varphi_1) + \Gamma^2} \]

\[ A_2(nk, \omega) = \frac{2\Gamma}{(\omega + V - \epsilon_{nk2} + \varphi_2) + \Gamma^2} \]

\[ n_F(\omega) = \frac{1}{1 + e^{\frac{(\omega - \mu)}{k_B T}}} \]

Dharmendar Reddy
Qualitative Capacitance and I-V for Graphene tunneling Device [SPICE model]

\[ V_{il} = V_{c1} - V_{c2} \quad \varphi_{il} = \varphi_1 - \varphi_2 \]

\[ V_{g1} = V_{gTop}; \quad V_{g2} = V_{gBot} \]

\[ C_{g1} = C_{g2} = C_g \]

\[ C_{il} = C_i \]

\[ \varphi_{il} = \frac{-C_g (V_{gTop} - V_{gBot}) + C_q (V_{il})}{C_g + C_i + 2C_q} \]

\[ I_{il} = A t^2 \beta_1 \frac{q^2 V_{il} (V_{il} - \varphi_2 - \beta_2 \varphi_1 - \beta_3)}{\Gamma^2 + \varphi_{il}^2} \]

Dharmendar Reddy
Graphene-to-graphene Interlayer Tunneling
Chris Corbet (Tutuc/Banerjee)

- No interlayer dielectric
- Independent Hall bar geometry on top and bottom flakes
- Channel width of 6µm
- Device length of 19µm
- Overlap area of 35 µm²
- Overlap area is device dependent
Results

- The effective fine structure constant in graphene parametrizes the interaction strength (suspended in vacuum $\alpha \sim 2.2$, good insulating substrates $\alpha > 1$):

\[ \alpha \equiv \frac{e^2}{\varepsilon \nu F} \]

* We employ a constant gap neglecting its frequency-momentum dependence in Dyson equation replacing it by its value at the Fermi surface, and use a high momentum cutoff of $2E_F$. 
MacDonald and Sinova have used full dynamic (retarded screening) in RPA to estimate the condensate gap ($\Delta$) as a function of the effective fine structure constant in graphene ($\alpha$), which depends on the coupling between the graphene layers. It shows that a condensate should exist at room temperature, unlike calculations based on static screening by other groups. Work by DasSarma has shown that disorder and electron-hole puddles can confound experimental data.
Four Bit Ripple Carry Adder

Total delay between input and output is $4 \times 7.5\text{p-sec} = 30\text{p-sec}$

(But can start with new input After 10 ps.)
Illustration of Gate Control on I-V

- **Vg1** = Vg
- **Vg2** = Vg
- $\Gamma$ = 2 meV
- $T_{\text{hop}}$ = 2 meV

- **Vg1** = Vg/2
- **Vg2** = -Vg/2
- $\Gamma$ = -Vg/2
- $T_{\text{hop}}$ = 2 meV

- **Vg1** = Vg
- **Vg2** = Vg
- $\Gamma$ = 25 meV
- $T_{\text{hop}}$ = 10 meV

- **Vg1** = Vg/2
- **Vg2** = -Vg/2
- $\Gamma$ = 25 meV
- $T_{\text{hop}}$ = 10 meV
Memory element

\[ V_{dd} \]

\[ \frac{W}{L} = 2 \]

\[ 25 \text{ mV} \]

\[ 12.5 \text{ mV} \]

\[ 25 \text{ mV} \]

Data

45
Write-1  Read-1  Write-0  Read-0

Tx
Data
Ac
Mem
BLine
Pc

Time (ns)
Multi-level logic & Clocking scheme

Requires multi-(4?)-phase clocking

A natural for pipelining: With output for each gate set, input can be released → new inputs processed each clock cycle no matter how many subsequent gates.